What is claimed is:

1. An apparatus comprising:

a plurality of processing units;

a monitor to obtain a plurality of monitor values from said plurality of processing units, wherein said monitor is to transfer a process from a first processing unit of said plurality of processing units to a second processing unit of said plurality of processing units in response to said plurality of monitor values.

2. The apparatus of claim 1 wherein said monitor is to transfer the process from the first processing unit to the second processing unit in response to a first one of said plurality of monitor values being greater than a second one of said plurality of monitor values over a period of time.

3. The apparatus of claim 2 wherein said monitor obtains a monitor value by at least one of the set consisting of:

receiving a temperature indicator;

estimating an activity level;

receiving a power consumption estimate.

4. The apparatus of claim 1 wherein each of said plurality of processing units is one of a set consisting of:

a core of a multi-core processor;

an execution unit of a processor;

a separate processor unit.

5. The apparatus of claim 1 wherein said monitor is further to increase and decrease a voltage level depending on a total power consumption or temperature level of said plurality of processing units.

6. The apparatus of claim 1 wherein said monitor comprises:

an exchange module to exchange processes between ones of said plurality of processing units.

7. The apparatus of claim 1 wherein said monitor comprises:

a move module to move one process from one of said plurality of processing units to another one of said plurality of processing units that is idle.

8. The apparatus of claim 6 wherein said monitor further comprises:

a move module to move one process from one of said plurality of processing units to another one of said plurality of processing units that is idle;

a sum module to throttle processing of one or more of said plurality of processing units if a sum total of power consumption of said plurality of processing units exceeds a selected total power consumption metric;

a shutdown module to shut down one or more of said plurality of processing units

in a low power mode.

9. The apparatus of claim 1 further comprising:

a cache coupled to said plurality of processing units, wherein said monitor is to swap processes between said first processing unit and said second processing unit by saving a first plurality of state variables from said first processing unit in said cache and saving a second plurality of state variables from said second processing unit in said cache and restoring said second plurality of state variables to said first processing unit from said cache and restoring said first plurality of state variables to said second processing unit from said cache.

10. The apparatus of claim 9 wherein said cache, said first processing unit, and said second processing unit are integrated on a single integrated circuit die, and wherein said cache is physically positioned between said first processing unit and said second processing unit.

11. The apparatus of claim 1 wherein said first processing unit and said second processing unit are coupled to receive power from different power wells and are capable of being independently operated at different voltages and frequencies under control of the monitor.

12. A multi-core processor comprising:

a first core having first instruction fetch and execute logic and a plurality of first

core state variables;

a second core having second instruction fetch and execute logic and a plurality of second core state variables;

a cache that is accessible to both said first core and said second core for read and write accesses;

a monitor to monitor temperature and/or power consumption of said first core and said second core, and, in response to a selected metric being reached by one of said first core and said second core, to trigger storage of said plurality of first core state variables and said plurality of second core state variables in said cache and restoring of said plurality of second core state variables to said first core and restoring of said plurality of first core state variables to said second core.

13. The multi-core processor of claim 12 wherein said first core and said second core are coupled to independently controllable power supplies which are controllable by said monitor.

14. The multi-core processor of claim 13 wherein said first core and said second core are independently operable at different frequencies under control of said monitor.

15. The multi-core processor of claim 14 wherein said selected metric comprises at least one of the set consisting of:

a level of processing activity;

a temperature level.

16. A system comprising:

a plurality of processing units, each processing unit to track its power consumption, and to support a process move procedure;

a monitor to receive monitor information from each of said plurality of processing units and to re-allocate processes to different ones of said plurality of processing units in response to the monitor information received from the plurality of processing units;

a memory coupled to said plurality of processing units to store instructions for execution by said plurality of processing units.

17. The system of claim 16 wherein said monitor comprises:

a power-aware scheduler to schedule tasks for specific ones of said plurality of processing units in response to said monitor information received from said plurality of processing units.

18. The system of claim 17 wherein said power-aware scheduler is chosen from the set consisting of:

an operating system scheduler that is stored in said memory during operation;

a hardware scheduler.

19. The system of claim 16 wherein said monitor comprises:

an exchange module to exchange processes between ones of said plurality of processing units;

a move module to move one process from one of said plurality of processing units to another one of said plurality of processing units that is idle;

a sum module to throttle processing of one or more of said plurality of processing units if a sum total of power consumption of said plurality of processing units exceeds a selected total power consumption metric;

a shutdown module to shut down one or more of said plurality of processing units in a low power mode.

20. A method comprising:

monitoring power consumption of a plurality of processing units;

swapping processes between said plurality of processing units in response to monitoring power consumption of said plurality of processing units.

21. The method of claim 20 wherein swapping comprises:

exchanging processor state data via a cache memory.

22. The method of claim 20 further comprising:

moving a process from a first one of said plurality of processing units to an idle one of said plurality of processing units in response to monitoring power consumption of said plurality of processing units.

23. The method of claim 21 further comprising:

reducing power consumption of one or more of said plurality of processing units in response to a sum of power consumed exceeding a selected total power consumption metric;

increasing power consumption of said plurality of processing units in response to the sum of power consumed being less than a second selected total power consumption metric.

24. The method of claim 23 further comprising:

periodically rearranging processes among said plurality of processing units.

25. The method of claim 20 further comprising:

independently controlling voltages and frequencies for said plurality of processing units in response to monitoring power consumption of the plurality of processing units.

26. An apparatus comprising:

a plurality of processing units;

a module to periodically transfer processes from a first processing unit from said plurality of processing units to a second processing unit from said plurality of processing units.

27. The apparatus of claim 26 further comprising a thermal monitor to independently control voltage levels of said plurality of processing units in response to a plurality of temperature levels of said plurality of processing units.

28. The apparatus of claim 27 wherein said thermal monitor is also to independently control clock frequencies for said plurality of processing units in response to said plurality of temperature levels.

29. An article comprising a machine readable medium storing a plurality of instructions which, if executed by a machine, cause the machine to perform operations comprising:

monitoring power consumption and/or thermal levels of a plurality of processing units;

swapping processes between said plurality of processing units in response to monitoring power consumption of said plurality of processing units.

30. The article of claim 29 wherein swapping comprises:

exchanging processor state data via a cache memory.

31. The article of claim 29 wherein said operations further comprise:

moving a process from a first one of said plurality of processing units to an idle one of said plurality of processing units in response to monitoring the power consumption of said plurality of processing units.

32. The article of claim 30 wherein said operations further comprise:

reducing power consumption of one or more of said plurality of processing units in response to a sum of power consumed exceeding a selected total power consumption metric;

increasing power consumption of said plurality of processing units in response to the sum of power consumed being less than a second selected total power consumption metric.

33. The article of claim 32 wherein said operations further comprise:

periodically rearranging processes among said plurality of processing units.

34. The article of claim 29 wherein said operations further comprise:

independently controlling voltages and frequencies for said plurality of processing units.

35. A method comprising:

monitoring temperature levels of a plurality of processing units;

swapping processes between said plurality of processing units in response to monitoring temperature levels of said plurality of processing units.

36. The method of claim 35 wherein swapping comprises:

exchanging processor state data via a cache memory.

37. The method of claim 35 further comprising:

periodically rearranging processes among said plurality of processing units.